PATENT
Attorney Docket No. JP920000112US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Takatoshi Tsujimura

Serial No: 09/681,643

Filed: May 15, 2001

For: METHOD AND APPARATUS FOR MANUFACTURING ACTIVE MATRIX DEVICE INCLUDING TOP GATE TYPE TFT

Examiner: William D. COLEMAN

Art Unit: 2823

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Respectfully submitted,

Dated: December 27, 2005

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APPEAL BRIEF

Board of Patent Appeals and Interferences
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The applicant submits this brief pursuant to 37 C.F.R. §1.192 in furtherance of the Notice of Appeal timely filed in this case on May 29, 2005, setting a two-month shortened statutory period of brief filing expiring July 29, 2005.

Please charge Deposit Account 50-0510 the $500 fee for filing this Appeal Brief. No other fee is believed due with this Appeal Brief, however, should another fee be required please charge Deposit Account 50-0510.

Real Party In Interest

The real party in interest is International Business Machines Corporation, as evidenced by the assignment set forth at Reel 012163, Frame 0482.

12/28/2005 TL0111 00000043 500510 09681643
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Related Appeals And Interferences

None.

Status of Claims

Claims 1-10 and 17-22 are pending in the present application, with claims 1 and 19 being independent claims. Claims 11-16 are cancelled.

Claims 1-10 and 17-21 stand finally rejected, as noted in the Final Office Action dated June 22, 2005("FOA"). The rejection of claims 1-10 and 17-22 is appealed herein.

Status of Amendments

No amendments to the claims were made after the final rejection.

Summary of the Claimed Subject Matter

During the conventional processing of a thin film transistor (TFT), chemical species containing P-type material (P) may remain in the chemical vapor deposition (CVD) processing chamber and can contaminate the formation of the TFT on a silicon wafer. App., ¶ 6. It is known that moving the wafer from a dirty chamber to a clean chamber can address this issue. App., ¶ 7. However, using a plurality of chambers for manufacturing of TFTs has various drawbacks. App., ¶ 8.

To address this issue, the present invention discloses a fabrication process that involves depositing an oxide layer, such as SiOx, onto the inner walls a processing chamber to prevent P-containing chemical species, such as phosphine (PH_3), from sticking to the CVD chamber walls. App., ¶ 25. According to one embodiment of the invention, coating the chamber inner walls is performed before P-doping, such as source and drain electrode

doping, takes place. App., ¶ 34. By introducing an oxide film on the inner walls of the processing chamber, contamination of the a-Si layer and the gate insulating film by P-containing chemicals subsequent to P-doping is reduced or eliminated. App., ¶ 32. Thus, the present invention beneficially allows P-doping, the formation of an a-Si layer, and a gate insulating film to be carried out in a single processing chamber. App., ¶ 32. In a particular embodiment of the invention, the thickness of the oxide film should preferably be set equal to 50 nm or higher, for example approximately 100 nm. App., ¶ 35.

Grounds for Rejection to be Reviewed on Appeal

I. Claims 1-10 and 17-22 are rejected under 35 USC §103 as obvious over U.S. Patent No. 6,072,193 to Ohnuma et al. ("Ohnuma") in view of U.S. Patent No. 6,066,519 to Gardner et al. ("Gardner").

II. There is no suggestion or motivation to combine the teachings of Ohnuma and Gardner.

III. Claim 22 has not been examined.

Argument

I. CLAIMS 1-10 AND 17-22 ARE NOT OBVIOUS OVER OHNUMA IN VIEW OF GARDNER

Claims 1-10 and 19-21 were rejected under 35 USC §103 as obvious over U.S. Patent No. 6,072,193 to Ohnuma et al. ("Ohnuma") in view of U.S. Patent No. 6,066,519 to Gardner et al. ("Gardner"). A *prima facie* case for obviousness can only be made if the combined reference documents teach or suggest all the claim limitations. MPEP 2143.

Claim 1

Claim 1 recites, in part, "forming an oxide film on an inner wall of a CVD processing chamber . . . wherein forming the oxide film on the inner wall of the CVD processing chamber is performed before doping the source and drain electrodes with P." The Appellants respectfully submit that neither Ohnuma nor Gardern teach or suggest forming an oxide film on the inner wall of the CVD processing chamber before doping the source and drain electrodes with P.

The Final Office Action alleges Ohnuma teaches wherein forming the oxide film on the inner wall of the CVD processing chamber is performed before doping the source and drain electrodes with P. FOA, pg. 6. The Final Office Action, however, also admits, "Ohnuma fails to disclose forming an oxide film on an inner wall of a CVD processing chamber." FOA, pg. 6. The Examiner has never explains how Ohnuma can teach forming an oxide film on an inner wall of the CVD processing chamber before doping the source and drain electrodes with P, yet fail to teach forming an oxide film on an inner wall of a CVD processing chamber.

The Appellants respectfully submit that Ohnuma makes no mention of forming an oxide film on the inner wall of the CVD processing chamber before doping the source and drain electrodes with P. Ohnuma relates to a TFT manufacturing process which suppresses residual metal elements on the TFT device characteristics. Ohnuma, col. 3, ln. 14-19. Ohnuma discloses various methods of forming and removing oxide films over the substrate and transistor elements. See, for example, Ohnuma, Figs. 1A-1E, items 102, 104, and 109. As the Examiner correctly points out, however, there is no teaching or suggestion in Ohnuma of forming an oxide film on an inner wall of a CVD processing chamber. The Appellants further contend that there is no teaching or suggestion of forming an oxide film on an inner wall of the CVD

processing chamber before doping the source and drain electrodes with P.

The Examiner also argues that in Fig. 3 of Gardner, step 306 of forming the SiO_x dielectric layer followed by step 308 of forming a second dielectric layer suggests "that cleaning the chamber takes place after the formation of forming the dielectric layers." FOA, pg. 3. The Appellants respectfully submit that claims 1, 19 and 22 do not recite forming the oxide film on the inner wall of the CVD processing chamber is performed before forming dielectric layers.

Moreover, it is submitted that Fig. 3, items 306 and 308, of Gardner do not teach or suggest forming an oxide film on an inner wall of the CVD processing chamber before doping the source and drain electrodes with P. Gardner clearly states, "A layer of oxide 403 is then formed over the substrate 401 using an oxide source showerhead as indicated at block 306" and "[a] second dielectric layer 405 may optionally be formed over the outgassed oxide layer 403 as indicated in block 308." Gardner, col. 4, ln. 54-55, col. 5, ln. 14-15 (emphasis added). Again, such a teaching cannot be equated to the limitation of forming the oxide film on the inner wall of the CVD processing chamber is performed before doping the source and drain electrodes with P, as recited in the pending claims.

The Examiner alleges that the Appellant is attacking references individually where the rejections are based on combined references. FOA, pg. 2. The Appellants respectfully submit, however, that a *prima facie* case for obviousness can only be made if the combined reference documents teach or suggest all the claim limitations. MPEP 2143. The Examiner has not supplied any reference in the record teaching or suggesting forming an oxide film on an inner wall of the CVD processing chamber before doping the source and drain electrodes with P.

Turning to another element of the claim, claim 1 recites, "forming an oxide film on an inner wall of a CVD processing chamber." The Final Office Action cites Gardner as teaching forming an oxide film on an inner wall of a CVD processing chamber at column 6, lines 8-14. FOA, pg. 6. The Appellant respectfully disagrees with the Examiner's interpretation of Gardner.

Gardner discloses, "The chamber may be cleaned by, for example, increasing the flow of NF_3 through the chamber in order to remove any residual oxide on the showerhead and/or chamber walls." Gardner, col. 6, ln. 10-13 (emphasis added). It is respectfully submitted that Gardner does not teach forming an oxide film on an inner wall of a CVD processing chamber, but rather removing an oxide layer on chamber walls that may have formed as a byproduct of substrate processing.

The Examiner argues, "Since cleaning normally is defined as removing something unwanted, the dielectric layer is removed from the chamber." FOA, pg. 3. The Appellant respectfully submit that removing possible residual oxide in the chamber does not teach or suggest actively forming an oxide film on an inner wall of a CVD processing chamber.

Thus, for at least these reasons, it is respectfully submitted that a *prima facie* case of obviousness under 35 USC §103 for claim 1 has not been made. Thus, the Appellant requests that the rejection of claim 1 be reversed by the honorable Board.

Claims 2-10, 17, 18 and 22

Claims 2-10, 17, 18 and 22 are dependent on and further limit claim 1. Since a *prima facie* case of obviousness has not been established for claim 1, the rejections of claims 2-10, 17, 18 and 22 are also improper.

Claim 19

Claim 19 recites, in part, "wherein forming the oxide film on the inner wall of the CVD processing chamber is performed before doping the source and drain electrodes with P." As discussed above for claim 1, the Appellants respectfully submit that neither Ohnuma nor Gardern teach or suggest forming an oxide film on the inner wall of the CVD processing chamber before doping the source and drain electrodes with P.

Claim 19 further recites, in part, "forming an oxide film on an inner wall of a CVD processing chamber, the oxide film being at least 50 nm thick." As discussed above for claim 1, the Appellants respectfully submit that neither Ohnuma nor Gardern teach or suggest forming an oxide film on the inner wall of the CVD processing chamber.

Furthermore, there is no teaching or suggestion in the cited art that the oxide film on an inner wall of the CVD processing chamber is at least 50 nm thick. The Examiner fails to show any appreciation in either Ohnuma or Gardern of an oxide film on an inner wall of the CVD processing chamber being is at least 50 nm thick. FOA, pg. 8.

In rejecting claim 20, the Examiner cites column 7, lines 9-10 of Ohnuma as allegedly disclosing a preferred oxide thickness. Ohnuma states, "Note that the film thickness of the pattern 108 may be less than or equal to 100 nm - preferably, 50 nm or less." Ohnuma, col. 7, ln. 9-10. The Examiner fails to appreciate, however, that this passage is describing the thickness of a silicon film, not an oxide film. Ohnuma, col. 7, ln. 6-8. Moreover, the silicon film discussed is deposited over the substrate, not on an inner wall of the CVD processing chamber.

Thus, for at least these reasons, it is respectfully submitted that a *prima facie* case of obviousness under 35 USC §103

for claim 19 has not been made. Thus, the Appellant requests that the rejection of claim 19 be reversed by the honorable Board.

Claim 20

Claim 20 is dependent on claim 19 and recites, "A manufacturing method of an active matrix device according to claim 19, wherein the oxide film is approximately 100 nm."

In rejecting claim 20, the Examiner cites column 7, lines 9-10 of Ohnuma as allegedly disclosing a preferred oxide thickness. Ohnuma states, "Note that the film thickness of the pattern 108 may be less than or equal to 100 nm - preferably, 50 nm or less." Ohnuma, col. 7, ln. 9-10. The Examiner fails to appreciate, however, that this passage is describing the thickness of a silicon film, not an oxide film. Ohnuma, col. 7, ln. 6-8. Moreover, the silicon film discussed is deposited over the substrate, not on an inner wall of the CVD processing chamber.

Thus, for at least this reason, and the reasons given for claim 19, it is respectfully submitted that a *prima facie* case of obviousness under 35 USC §103 for claim 20 has not been made. Thus, the Appellant requests that the rejection of claim 20 be reversed by the honorable Board.

Claim 21

Claim 21 is dependent on and further limits claim 19. Since a *prima facie* case of obviousness has not been established for claim 19, the rejection of claim 21 is also improper.

II. THERE IS NO SUGGESTION OR MOTIVATION TO COMBINE THE TEACHINGS OF OHNUMA AND GARDNER

To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. *See* MPEP 2143 *et seq*. Obviousness cannot be

established by combining prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *In re Fritch*, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992). The mere fact that the prior art may be modified in the manner suggested by an Examiner does make the modification obvious unless the prior art suggested the desirability of the modification. *Id.*

In the present case, the advantage alleged by the Examiner to justify the proposed combination of Ohnuma and Gardner does not stand up to close scrutiny. More particularly, the examiner has not explained, and it not evident, why a person of ordinary skill in the art would have found it obvious to reconstruct Ohnuma to form an oxide film on an inner wall of a CVD processing chamber, wherein forming the oxide film on the inner wall of the CVD processing chamber is performed before doping the source and drain electrodes with P. FOA, pg. 6.

In this regard, neither Ohnuma nor Gardner express any appreciation of seasoning or pre-coating the inner wall of the processing chamber with an oxide film so as to prevent the chemical species containing P from being stuck to the inner wall thereof, as attributed in the Applicant's specification. Thus, it is apparent that the only suggestion for combining Ohnuma and Gardner in the manner advanced by the Examiner stems from hindsight knowledge impermissibly derived from the Appellant's disclosure.

Thus, for at least these reasons, it is respectfully submitted that a *prima facie* case of obviousness under 35 USC §103 for claims 1-10 and 19-21 has not been made. The Appellant requests that the rejections of claims 1-10 and 19-21 be reversed by the honorable Board.

III. CLAIM 22 HAS NOT BEEN EXAMINED

Claim 22 was introduced to the present Application in an Amendment and Response to Office Action Dated January 21, 2005, filed April 15, 2005. The Final Office Action does not address the merits of claim 22 and a *prima facie* case of unpatentability for claim 22 has not been made.

Conclusion

In view of the foregoing, Appellant submits that the rejections of claims 1-10 and 17-22 are improper and respectfully requests that the rejections of claims 1-10 and 17-22 be reversed by the Board.

Respectfully submitted,

Dated: December 27, 2005

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Claims Appendix

Claim 1. (previously presented) A manufacturing method of an active matrix device including a top gate type TFT, which comprises a process of forming the top gate type TFT, wherein the process of forming the top gate type TFT includes the steps of:

forming an oxide film on an inner wall of a CVD processing chamber;

arranging a substrate having source and drain electrodes formed therein in the processing chamber;

doping the source and drain electrodes with P;

forming an a-Si layer and a gate insulating film in the processing chamber; and

wherein forming the oxide film on the inner wall of the CVD processing chamber is performed before doping the source and drain electrodes with P.

Claim 2. (original) A manufacturing method of an active matrix device according to claim 1, wherein the process of forming the top gate type TFT further comprises the step of removing the oxide film from the inner wall after the step of forming the a-Si layer and the gate insulating film.

Claim 3. (original) A manufacturing method of an active matrix device according to claim 1, wherein the oxide film contains SiOx.

Claim 4. (original) A manufacturing method of an active matrix device according to claim 1, wherein the active matrix device is a liquid crystal display.

Claim 5. (original) A manufacturing method of an active matrix device according to claim 1, wherein the active matrix device is an electroluminescence display.

Claim 6. (original) A manufacturing method of an active matrix device according to claim 2, wherein the oxide film contains SiOx.

Claim 7. (original) A manufacturing method of an active matrix device according to claim 2, wherein the active matrix device is a liquid crystal display.

Claim 8. (original) A manufacturing method of an active matrix device according to claim 3, wherein the active matrix device is a liquid crystal display.

Claim 9. (original) A manufacturing method of an active matrix device according to claim 2, wherein the active matrix device is an electroluminescence display.

Claim 10. (original) A manufacturing method of an active matrix device according to claim 3, wherein the active matrix device is an electroluminescence display.

Claims 11-16 (cancelled)

Claim 17. A manufacturing method of an active matrix device according to claim 1, further comprising heating the inner wall of the CVD processing chamber.

Claim 18. A manufacturing method of an active matrix device according to claim 1, wherein the oxide film is selected from the group consisting of SiOx, Al_2O_3, TiO_2, $Al_2(Si_2O_5)(OH)_4$, $MgAl_2O_4$, TaOx, and ZrOx.

Claim 19. A manufacturing method of an active matrix device including a top gate type TFT, which comprises a process of forming the top gate type TFT, wherein the process of forming the top gate type TFT includes the steps of:

forming an oxide film on an inner wall of a CVD processing chamber, the oxide film being at least 50 nm thick;

arranging a substrate having source and drain electrodes formed therein in the processing chamber;

doping the source and drain electrodes with P;

forming an a-Si layer and a gate insulating film in the processing chamber; and

wherein forming the oxide film on the inner wall of the CVD processing chamber is performed before doping the source and drain electrodes with P.

Claim 20. A manufacturing method of an active matrix device according to claim 19, wherein the oxide film is approximately 100 nm.

Claim 21. A manufacturing method of an active matrix device according to claim 19, wherein forming the oxide film on the inner wall of the CVD processing chamber is performed before doping the source and drain electrodes with P.

Claim 22. A manufacturing method of an active matrix device according to claim 1, further comprising:

depositing a first gate insulating film;

forming the drain and source electrodes after depositing the first gate insulating film before forming the oxide film on the inner wall of the CVD processing chamber

depositing a second gate insulating film after forming the a-Si layer;

removing the oxide film after depositing the second gate insulating film;

wherein forming the oxide film on the inner wall of the CVD processing chamber is performed before doping the source and drain electrodes with P; and

wherein doping the source and drain electrodes, forming the a-Si layer, and depositing the second gate insulating film is carried out in the CVD processing chamber.